ABSTRACT OF THE DISCLOSURE

A complementary output stage in integrated circuit includes a P-channel transistor (MP1) the segmented into a first group of sections (MP1-1,2...12) and an N-channel transistor (MN1) segmented into a second group of sections (MN1-1,2...12). The sections of the first group are disposed in a plurality of N-type well regions (35), respectively, and the sections of the second group are disposed in a plurality of P-type well regions (36), respectively. The sections of the first group are alternately located with respect to the sections of the second group so as to form an interdigitated output stage area of the integrated circuit including the P-channel transistor (MP1) and the N-channel transistor (MN1) so that the higher amount of heat normally generated in the N-channel transistor is dissipated over the entire interdigitated output stage area and reduces peak temperatures in the N-channel transistor.